

What is claimed is:

- 1           1.     A memory device comprising:  
2                 a substrate; and  
3                 a single transistor formed on the substrate, the transistor having a  
4                 gate with a nonvolatile memory element.
- 1           2.     The memory device of claim 1, wherein the nonvolatile memory  
2                 element is formed between a gate insulating layer and a gate conductive  
3                 layer, both layers constituting the gate.
- 1           3.     The memory device of claim 1, wherein the nonvolatile memory  
2                 element is connected to first and second bit lines separated from each other.
- 1           4.     The memory device of claim 3, wherein the first and second bit  
2                 lines pass below the nonvolatile memory element.
- 1           5.     The memory device of claim 3, wherein the first and second bit  
2                 lines pass above the nonvolatile memory element.
- 1           6.     The memory device of claim 1, wherein the nonvolatile memory  
2                 element includes:  
3                     semiconductor quantum dots formed on the gate insulating layer; and  
4                     an amorphous material layer covering the plurality of semiconductor  
5                     quantum dots, wherein the amorphous material layer stores carriers emitted  
6                     from the semiconductor quantum dots and maintains the carriers in a  
7                     nonvolatile state until the emitted carriers are recaptured into the  
8                     semiconductor quantum dots.
- 1           7.     The memory device of claim 6, wherein the semiconductor  
2                 quantum dots are silicon dots arranged at regular intervals.

1           8.     The memory device of claim 6, wherein the amorphous  
2 material layer, which is an amorphous dielectric layer, is an amorphous  
3 silicon nitride layer, an amorphous alumina layer or a silicon oxide layer  
4 ( $\text{SiO}_2$ ).

1           9.     The memory device of claim 2, wherein the nonvolatile memory  
2 element includes:  
3           semiconductor quantum dots formed on the gate insulating layer; and  
4           an amorphous material layer covering the plurality of semiconductor  
5 quantum dots, wherein the amorphous material layer stores carriers emitted  
6 from the semiconductor quantum dots and maintains the carriers in a  
7 nonvolatile state until the emitted carriers are recaptured into the  
8 semiconductor quantum dots.

1           10.    The memory device of claim 9, wherein the semiconductor  
2 quantum dots are silicon dots arranged at regular intervals.

1           11.    The memory device of claim 9, wherein the amorphous  
2 material layer, which is an amorphous dielectric layer, is an amorphous  
3 silicon nitride layer, an amorphous alumina layer or a silicon oxide layer  
4 ( $\text{SiO}_2$ ).

1           12.    The memory device of claim 3, wherein the nonvolatile  
2 memory element includes:  
3           semiconductor quantum dots formed on the gate insulating layer; and  
4           an amorphous material layer covering the plurality of semiconductor  
5 quantum dots, wherein the amorphous material layer stores carriers emitted  
6 from the semiconductor quantum dots and maintains the carriers in a  
7 nonvolatile state until the emitted carriers are recaptured into the  
8 semiconductor quantum dots.

1           13.    The memory device of claim 12, wherein the semiconductor  
2 quantum dots are silicon dots arranged at regular intervals.

1           14.    The memory device of claim 12, wherein the amorphous  
2           material layer, which is an amorphous dielectric layer, is an amorphous  
3           silicon nitride layer, an amorphous alumina layer or a silicon oxide  
4           layer(SiO<sub>2</sub>).

1           15.    The memory device of claim 4, wherein the nonvolatile memory  
2           element includes:

3                   semiconductor quantum dots formed on the gate insulating layer; and  
4                   an amorphous material layer covering the plurality of semiconductor  
5           quantum dots, wherein the amorphous material layer stores carriers emitted  
6           from the semiconductor quantum dots and maintains the carriers in a  
7           nonvolatile state until the emitted carriers are recaptured into the  
8           semiconductor quantum dots.

1           16.    The memory device of claim 15, wherein the semiconductor  
2           quantum dots are silicon dots arranged at regular intervals.

1           17.    The memory device of claim 15, wherein the amorphous  
2           material layer, which is an amorphous dielectric layer, is an amorphous  
3           silicon nitride layer, an amorphous alumina layer or a silicon oxide layer  
4           (SiO<sub>2</sub>).

1           18.    The memory device of claim 5, wherein the nonvolatile memory  
2           element includes:

3                   semiconductor quantum dots formed on the gate insulating layer; and  
4                   an amorphous material layer covering the plurality of semiconductor  
5           quantum dots, wherein the amorphous material layer stores carriers emitted  
6           from the semiconductor quantum dots and maintains the carriers in a  
7           nonvolatile state until the emitted carriers are recaptured into the  
8           semiconductor quantum dots.

1           19.    The memory device of claim 18, wherein the semiconductor  
2           quantum dots are silicon dots arranged at regular intervals.

1           20.    The memory device of claim 18, wherein the amorphous  
2           material layer, which is an amorphous dielectric layer, is an amorphous  
3           silicon nitride layer, an amorphous alumina layer or a silicon oxide layer  
4           (SiO<sub>2</sub>).

1           21.    The memory device of claim 4, wherein the first and second bit  
2           lines are conductive impurity layers formed from the surface of the substrate  
3           to a predetermined depth.

1           22.    The memory device of claims 3, wherein a sense amplifier is  
2           connected to the first bit line as a current measuring means.

1           23.    The memory device of claim 4, wherein a sense amplifier is  
2           connected to the first bit line as a current measuring means.

1           24.    The memory device of claim 5, wherein a sense amplifier is  
2           connected to the first bit line as a current measuring means.

1           25.    The memory device of claim 21, wherein a sense amplifier is  
2           connected to the first bit line as a current measuring means.

1           26.    A semiconductor memory device comprising:  
2           a substrate;  
3           a transistor formed on the substrate; and  
4           a nonvolatile memory means formed between the transistor and the  
5           substrate.

1           27.    The semiconductor memory device of claim 26, wherein the  
2           nonvolatile memory means includes an amorphous material layer formed on  
3           the substrate and semiconductor quantum dots formed on the amorphous  
4           material layer, wherein the amorphous material layer stores carriers emitted  
5           from the semiconductor quantum dots and maintains the carriers in a

6 nonvolatile state until the emitted carriers are recaptured into the  
7 semiconductor quantum dots.

1 28. The semiconductor memory device of claim 27, wherein the  
2 transistor comprises:

3 first and second metal layer patterns formed on the amorphous  
4 material layer, both being separated from each other;

5 an insulating layer formed on the amorphous material layer so as to  
6 cover the semiconductor quantum dots and the first and second metal  
7 layers;

8 and a word line formed on the insulating layer at a position  
9 corresponding to a position where the semiconductor quantum dots are  
10 formed.

1 29. The semiconductor memory device of claim 27, wherein the  
2 semiconductor quantum dots are a plurality of spaced silicon dots.

1 30. The semiconductor memory device of claim 27, wherein the  
2 amorphous material layer, which is an amorphous dielectric layer, is an  
3 amorphous silicon nitride layer, an amorphous alumina layer or a silicon  
4 oxide layer (SiO<sub>2</sub>).

1 31. The semiconductor memory device of claim 28, wherein the  
2 semiconductor quantum dots are a plurality of spaced silicon dots.

1 32. The semiconductor memory device of claim 28, further  
2 comprising:

3 an interlayer dielectric layer formed on the insulating layer for  
4 covering the word line;

5 a via hole formed in the interlayer dielectric layer and the insulating  
6 layer so that the first metal pattern is exposed; and

7 a fourth metal layer pattern formed on the interlayer dielectric layer for  
8 filling the via hole and passing across the word line.

1           33.    A method for operating a memory device including a single  
2 transistor formed on a substrate, wherein the single transistor is a memory  
3 transistor having a gate with a nonvolatile memory element, and the  
4 nonvolatile memory element is connected to a bit line comprised of first and  
5 second bit lines passing across the gate, wherein an addressing voltage and  
6 a write voltage are applied to the gate and the bit line, respectively, to write  
7 data to the nonvolatile memory element.

1           34.    The method of claim 33, wherein first and second write  
2 voltages are applied to the first and second bit lines, respectively, to store  
3 data "1" and "0" to the nonvolatile memory element, and the first and second  
4 write voltages are the same as or different from each other.

1           35.    The method of claim 33, wherein a second write voltage is  
2 applied to the first bit line to store data "1", a first write voltage is applied  
3 to the second bit line to store data "0", and the first and second write  
4 voltages are the same as or different from each other.

1           36.    The method of claim 33, wherein a first write voltage is applied  
2 to the second bit line to store data, and a second write voltage higher than  
3 the first write voltage is applied to the second bit line to store different data.

1           37.    The method of claim 33, wherein the written data is read by  
2 measuring the conductivity of the nonvolatile memory element.

1           38.    The method of claim 37, wherein an addressing voltage is  
2 applied to the gate, and then a current measuring means is connected to the  
3 first bit line to measure current between the gate and the first bit line and  
4 thus the conductivity of the nonvolatile memory element.

1           39.    The method of claim 38, wherein data "1" or data "0" is read  
2 depending on the measured current.

1           40.    A method for operating a memory device including a substrate,  
2           a transistor formed on the substrate, the transistor having a gate, a drain  
3           connected to a bit line, and a source connected to a source of another  
4           transistor, a nonvolatile memory element formed between the gate and the  
5           substrate, and a metal line parallel to a word line connected to the transistor,  
6           wherein data is written by changing the conductivity of the nonvolatile  
7           memory element when the metal line is grounded.

1           41.    The method of claim 40, wherein the nonvolatile memory  
2           element is comprised of a material layer for storing carriers, and  
3           semiconductor quantum dots formed thereon.

1           42.    The method of claim 41, wherein a write voltage and an  
2           addressing voltage are applied to the bit line and the word line, respectively,  
3           when the metal line is grounded, to write data by changing the conductivity  
4           of the carrier storing material layer.

1           43.    The method of claim 42, wherein data is written by changing  
2           the addressing voltage while the write voltage remains constant.

1           44.    The method of claim 42, wherein data is written by changing  
2           the write voltage while the addressing voltage remains constant.

1           45.    The method of claim 40, wherein the written data is read by  
2           measuring the conductivity of the nonvolatile memory element.

1           46.    The method of claim 45, wherein a read voltage is applied to  
2           the bit line, and then a current measuring means is connected to the metal  
3           line to measure current between the bit line and the metal line and thus the  
4           conductivity of the nonvolatile memory element.

1           47.    The method of claim 46, wherein a different first or second  
2   read voltage is applied to the bit line to measure current between the bit line  
3   and the metal line and thus read data.

1           48.    The method of claim 45, wherein a read voltage and an  
2   addressing voltage are applied to the metal line and the word line,  
3   respectively, and then a current measuring means is connected to the bit line  
4   to measure current between the metal line and the bit line and thus the  
5   conductivity of the nonvolatile memory element.

1           49.    The method of claim 47, wherein data "0" is read when  
2   the measured current is large and the data "1" is read when the measured  
3   current is small.

1           50.    The method of claim 48, wherein data "0" is read when  
2   the measured current is large and the data "1" is read when the measured  
3   current is small.

1           51.    A method of manufacturing a memory device comprising:  
2           defining a field region and an active region in a substrate;  
3           forming a field oxide layer on the field region;  
4           forming an insulating layer on the active region;  
5           patterning the insulating layer to form first and second bit lines  
6   separated from and parallel to each other on the active region;  
7           forming a memory element for storing data in a nonvolatile state on  
8   the insulating layer and the first and second bit lines so that the memory  
9   element passes across the first and second bit lines; and  
10          forming a word line on the insulating layer and the memory element.

1           52.    The method of claim 51, wherein the step of forming the  
2   memory element further comprises:  
3           forming a plurality of spaced semiconductor quantum layers on the  
4   insulating layer and the first and second bit lines; and



5 forming an amorphous material layer covering the semiconductor  
6 quantum dots on the insulating layer.

1 53. The method of claim 51, wherein the step of forming the  
2 memory element comprises:  
3 forming an amorphous material layer on the insulating layer and the first  
4 and second bit lines; and  
5 forming spaced semiconductor quantum dots on the amorphous  
6 material layer.

1 54. The method of claim 52, wherein the amorphous material layer  
2 is an amorphous dielectric layer.

1 55. The method of claim 54, wherein the amorphous dielectric  
2 layer is formed of an amorphous silicon nitride layer, an amorphous alumina  
3 layer or a silicon oxide layer ( $\text{SiO}_2$ ).

1 56. The method of claim 53, wherein the amorphous material layer  
2 is an amorphous dielectric layer.

1 57. The method of claim 56, wherein the amorphous dielectric  
2 layer is formed of an amorphous silicon nitride layer, an amorphous alumina  
3 layer or a silicon oxide layer ( $\text{SiO}_2$ ).

1 58. The method of claim 52, wherein the semiconductor quantum  
2 dots are silicon dots for emitting carriers to the amorphous material layer or  
3 recapturing the emitted carriers by application of a voltage.

1 59. The method of claim 53, wherein the semiconductor quantum  
2 dots are silicon dots for emitting carriers to the amorphous material layer or  
3 recapturing the emitted carriers by application of a voltage.

1           60.    A method of manufacturing a memory device, the method  
2 comprising:  
3           forming a nonvolatile amorphous material layer on a substrate; and  
4           forming a transistor on the nonvolatile amorphous material layer so  
5 that semiconductor quantum dots for emitting carriers to the amorphous  
6 material layer or recapturing the emitted carriers by application of a voltage  
7 are formed between the transistor and the amorphous material layer.

1           61.    The method of claim 60, wherein the step of forming the  
2 transistor comprises:  
3           forming first and second metal layer patterns on the nonvolatile  
4 amorphous material layer;  
5           forming semiconductor quantum dots on the nonvolatile amorphous  
6 material layer between the first and second metal layer patterns;  
7           forming a gate insulating layer covering the resultant in which the  
8 semiconductor quantum dots are formed on the substrate; and  
9           forming a word line corresponding to the semiconductor quantum dots  
10 on the gate insulating layer.

1           62.    The method of claim 60, wherein the nonvolatile amorphous  
2 material layer is formed of an amorphous silicon nitride layer, an amorphous  
3 alumina layer or a silicon oxide layer ( $\text{SiO}_2$ ).

1           63.    The method of claim 60, wherein the semiconductor quantum  
2 dots are silicon dots.

1           64.    The method of claim 61, further comprising:  
2           forming an interlayer dielectric layer covering the word line on the  
3 gate insulating layer;  
4           forming a via hole for exposing the first metal layer pattern; and  
5           forming a fourth metal layer pattern for filling the via hole and passing  
6 across the word line on the interlayer dielectric layer.